REMARKS

Upon entry of this Amendment, which amends Claim 1, Claims 1-11 remain pending in the present application. In the February 18, 2003 Office Action, Claims 1, 2 and 4-6 were rejected under 35 U.S.C. § 102(e), as allegedly being anticipated by U.S. Patent No. 5,821,769 to Douseki (hereinafter referred to as "Douseki"); Claim 3 was rejected under 35 U.S.C. § 103, as allegedly being unpatentable over Douseki in view of International Publication No. WO 96/07205 to Hu et al.; and Claims 7-11 were rejected under35 U.S.C. § 103, as allegedly being unpatentable over Douseki in view of U.S. Patent No. 6,015,993 to Voldman et al. Applicant respectfully requests reconsideration of the claims in view of the above amendments and the comments below.

35 U.S.C. § 102 Claim Rejections – Claims 1, 2 and 4-6

On pages 2-3 of the February 18, 2003 Office Action, Claim 1, 2 and 4-6 were rejected under 35 U.S.C. § 102, as allegedly being anticipated by Douseki. For the following reasons, Applicant respectfully disagrees.

Douseki discloses a MOSFET circuit 112, which can achieve high speeds of operation while consuming low power over a wide supply voltage range. FIGS. 9A and 9B of Douseki, in particular, shows a cross-sectional view of the MOSFET circuit 112 formed on a silicon subsrate 31. As shown in those figures, it is important to notice that doped regions 25 and 26 are not in physical contact with one another.

Independent Claim 1 of the present invention claims a semiconductor device, comprising: a first dynamic threshold voltage MOS transistor having a gate and a channel of a first conductivity type; a first doped zone of the first conductivity type coupled to the channel of said first MOS transistor; and a current limiter coupled between the gate of said first MOS transistor and said first doped zone. Claim 1 also recites how the current limiter comprises "*a second doped zone of a second conductivity type*", which is "*physically disposed against said first doped zone*".

Comparing Claim 1 of the present invention to Douseki reveals that Douseki does not disclose a semiconductor device having "a second doped zone of a second conductivity type", which is "*physically disposed against said first doped zone*". In other words, in Douseki the doped region 25 (designated in the Office Action as corresponding to the "first doped zone") and doped region 26 (designated in the Office Action as corresponding to the "second doped zone") are not "physically disposed against" one another, as Claim 1 requires. Doped regions 25 and 26 in Douseki are physically separated by at least the body 24 of transistor M2 and by the buried oxide layer 32. For at least this reason, Douseki does not teach each and every limitation of Claim 1. Consequently, Douseki does not anticipate Claim 1. Applicant respectfully requests, therefore, that the § 102 rejection of Claim 1, as allegedly being anticipated by Douseki, be withdrawn.

All of the remaining claims in the present application, i.e. Claims 2-11, depend from independent Claim 1, which as described above is allowable over Douseki. Applicant requests, therefore, that the § 102 rejections of Claim 2-11, as allegedly being

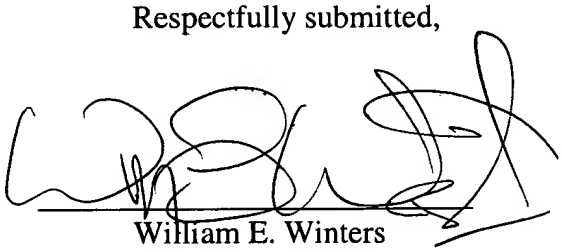
anticipated by Douseki, be withdrawn as being claims that depend from an allowable base claim.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 408-282-1857.

Respectfully submitted,



Dated: July 11, 2003

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